device including a controller for controlling data input/output of an associative memory, wherein the controller fetches an address and data that are transferred between a **second** device and a **third** device that are connected only on the system bus so as to duplicate and store them in the associative memory, as required by claims 1, 6, and 11-14. West teaches an IOP (60) that includes an IOP microprocessor (44, rejection equates to the claimed controller), an IOP local memory (46, rejection equates to the claimed associative memory), and a cache memory (62, rejection seems to also equate to the claimed associative memory). However, West teaches that the IOP local memory (46) only fetches address and data when transferring between its **own** IOP (60, rejection equates to the claimed first device) and another IOP (60, rejection equates to the claimed second device). West does not teach that either the IOP local memory (46) or the cache (memory) stores or buffers address and data transferred between two other IOPs provided off of the system bus (28), as is required by claims 1, 6, and 11-14. In fact, the purpose of the IOP taught by West is to mirror what is contained in the attached storage device (22, rejection equates to the claimed fourth device). See Figure 2.

Even further, claims 1, 6, and 11 require an associative memory from which a controller reads out data so as to transfer it to the local bus upon a request by a fourth device off of the local bus, where the requested read address is associated with one of the second and third devices on the system bus and the read address is contained in the address stored in the associative memory. (Method claims 12-14 require a buffering operation.) West teaches that only the IOP expansion bus (36, rejection equates to the claimed local bus) is consumed during data transfers, and that the IOP local bus (42), to which the IOP local memory (46) is also attached, is not used. Therefore, West teaches that during a transfer, address and data is not transferred from the IOP local memory (46). In fact, the cache memory (62) taught by West is provided specifically so that the IOP local memory (46) does not have to be involved with data transfers (see column 7, lines 14-17). Therefore, the IOP local memory (46) cannot be considered equivalent to the claimed associative memory.

Even further, claims 1, 6, and 11-14 require that a **fourth device on the local bus generates a read cycle** to read data from a read address associated with one of the second and third devices on the system bus and the read address is contained in the address stored in the

associative memory, the controller reads out corresponding data from the associative memory so as to **transfer it to the local bus**. However, West teaches that a host processor (30) provided off of the **system bus** requests data transfers, upon which the address/data is **transferred to the system bus**. See column 3, lines 6-7.

Even if one were to consider the IOP expansion bus (36) taught by West as being equivalent to the claimed system bus, and the connection between the storage device (22) and the I/O adapter (48) as equivalent to the claimed local bus, West still would not meet the requirements of claims 1, 6, and 11-14. The cache memory (62) is not provided between the connection between the storage device (22) and the I/O adapter (48) and the IOP expansion bus (36). Further, any data transferred from the cache memory (62) at the request of the storage device (22) would travel over the IOP expansion bus (36, which in this scenario is equivalent to the claimed system bus). In contrast, claims 1, 6, and 11-14 required that corresponding data from the associative memory is transferred to the local bus, thereby preventing bandwidth on the system bus from being utilized.

Favorable reconsideration of claims 1-14 is requested.

In view of the above, favorable reconsideration in the form of a notice of allowance is requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612)455-3804.

Respectfully Submitted,

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